[0164] In an example, the method further comprises: receiving a second feedback voltage from a second voltage rail coupled to a second load circuit of the plurality of load circuits; comparing the second feedback voltage to a second reference voltage; and based on the comparison, controlling a second switch connection circuit to couple the charge storage device to the second voltage rail for a second portion of the arbitration round, where the second switch connection circuit is associated with the second load circuit.

[0165] In another example, a computer readable medium including instructions is to perform the method of any of the above examples.

[0166] In another example, a computer readable medium including data is to be used by at least one machine to fabricate at least one integrated circuit to perform the method of any one of the above examples.

[0167] In another example, an apparatus comprises means for performing the method of any one of the above examples.

[0168] In another example, a system comprises: a processor including: a first die having a plurality of cores, at least one cache memory, and at least one I/O interface; and a second die having an integrated voltage regulator. In turn, the integrated voltage regulator may comprise: a switch capacitor circuit to receive a first voltage and charge at least one capacitor with the first voltage in a first phase and output charge in a second phase; a selection circuit coupled to the switch capacitor circuit to couple the output charge to a selected one of a plurality of voltage rails coupled to the first die according to a power arbitration; and a control circuit to perform the power arbitration, based at least in part on feedback information from one or more of the plurality of voltage rails. The system may further include a system memory coupled to the processor.

[0169] In an example, the control circuit comprises an arbiter to perform the power arbitration, to cause the output charge to be provided to one or more of the plurality of voltage rails in an arbitration round, where the arbiter is to cause the output charge to be provided to a first voltage rail based on a comparison of a feedback voltage of the first voltage rail to a first reference voltage.

[0170] In an example, the arbiter is to provide the output charge to the first voltage rail in a plurality of portions of the arbitration round, based at least in part on a priority of a first load circuit coupled to the first voltage rail.

[0171] In an example, the switch capacitor circuit comprises: a first switch to switchably provide the first voltage to a first capacitor; and a second switch to switchably couple the first capacitor to a second capacitor, where in the first phase, the first switch and the second switch are to cause the first and second capacitors to be charged with the first voltage.

[0172] In an example, the selection circuit comprises a plurality of switch connection circuits each to couple the first and second capacitors to a corresponding one of the plurality of voltage rails in the second phase, when enabled.

[0173] Understand that various combinations of the above examples are possible.

[0174] Embodiments may be used in many different types of systems. For example, in one embodiment a communication device can be arranged to perform the various methods and techniques described herein. Of course, the scope of the present invention is not limited to a communication device, and instead other embodiments can be directed to other types of apparatus for processing instructions, or one or more machine readable media including instructions that in response to being executed on a computing device, cause the device to carry out one or more of the methods and techniques described herein.

[0175] Embodiments may be implemented in code and may be stored on a non-transitory storage medium having stored thereon instructions which can be used to program a system to perform the instructions. Embodiments also may be implemented in data and may be stored on a non-transitory storage medium, which if used by at least one machine, causes the at least one machine to fabricate at least one integrated circuit to perform one or more operations. The storage medium may include, but is not limited to, any type of disk including floppy disks, optical disks, solid state drives (SSDs), compact disk read-only memories (CD-ROMs), compact disk rewritables (CD-RWs), and magneto-optical disks, semiconductor devices such as read-only memories (ROMs), random access memories (RAMs) such as dynamic random access memories (DRAMs), static random access memories (SRAMs), erasable programmable read-only memories (EPROMs), flash memories, electrically erasable programmable read-only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions.

[0176] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A processor comprising:

a plurality of cores;

a plurality of load circuits;

a first voltage regulator to provide an operating voltage to one or more of the plurality of cores;

a power switcher circuit to receive a first voltage and charge at least one charge storage device with the first voltage in a first phase and output charge in a second phase;

a selection circuit coupled to the power switcher circuit, the selection circuit to couple the output charge to a selected one of the plurality of load circuits responsive to a control signal; and

a control circuit to generate the control signal based at least in part on a comparison of a feedback voltage of a rail coupled to the selected load circuit to a reference voltage.

2. The processor of claim **1**, wherein the control circuit comprises an arbiter to provide the output charge to one or more of the plurality of load circuits in an arbitration round.

3. The processor of claim **2**, wherein the arbiter is to provide the output charge to a first load circuit when the feedback voltage of a first rail coupled to the first load circuit is less than a first reference voltage.

4. The processor of claim **2**, wherein the arbiter is to provide the output charge to a first load circuit in a plurality of portions of the arbitration round, the first load circuit having a first priority.

5. The processor of claim **2**, wherein the arbiter is to prevent the output charge from being provided to a first load circuit, when the first load circuit is in a low power state.